

**DLC Display Co., Limited**

德爾西顯示器有限公司



MODEL No: DLC0169ANOF

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### Record of Revision

Date	Revision No.	Summary
2010-05-29	1.0	Rev 1.0 was issued

## 1. Scope

This data sheet is to introduce the specification of DLC0169ANOF, passive matrix OLED module. It is composed of an OLED panel, driver ICs. The 1.69" display area contains 160(RGB) x 128 pixels.

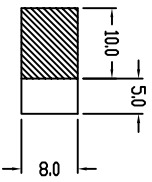
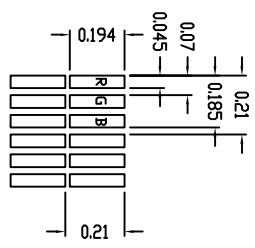
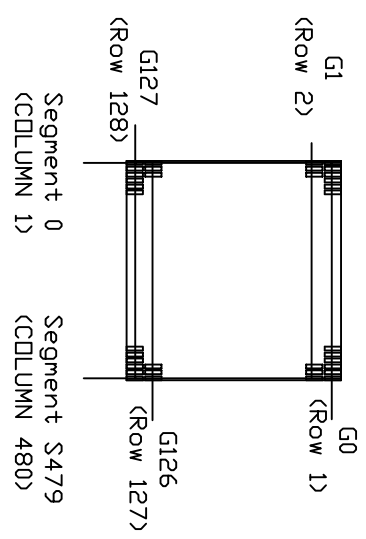
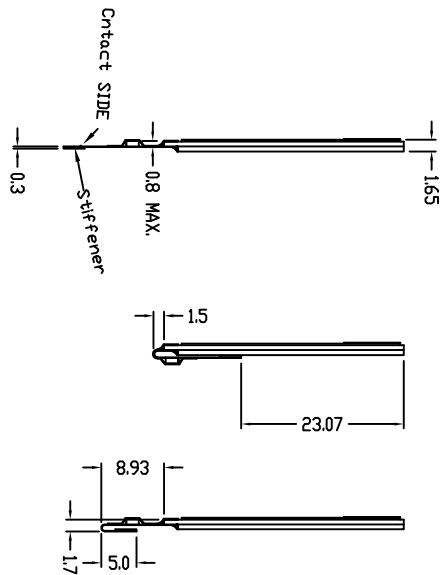
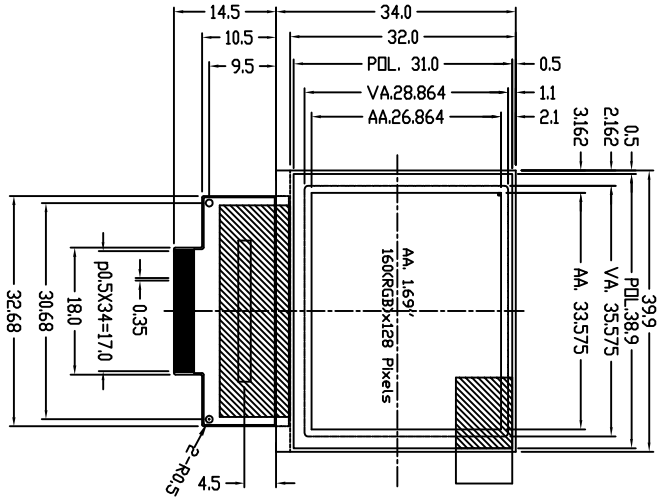
## 2. Application

Digital equipments which need color display, mobile phone, mobile navigator/video systems.

## 3. General Information

Item	Contents	Unit
Size	1.69	inch
Resolution	160(RGB) x 128	/
Technology type	Passive OLED	/
Display Color	262,144 Colors (Maximum)	
Interface	CPU/RGB	
Pixel pitch	0.07x0.21	mm
Pixel Configuration	R.G.B. Vertical Stripe	
Outline Dimension (W x H x D)	39.90 x 34.00 x 1.70	mm
Active Area	33.575 x 26.864	mm
Display Mode	Passive Matrix	/
Drive Duty	1/128 Duty	/
Driver IC	SEPS525-F00	
Operating Temperature	-30°C~+70°C	
Storage Temperature	-40°C~+80°C	

No.	PIN NAME
1	NC
2	VSDH
3	VDDH
4	VSSH
5	REF
6	DSCA2
7	DSCA1
8	VDDID
9	VSNCD
10	VSNVC
11	HSVNC
12	DOTCLK
13	ENABLE
14	CPU
15	PS
16	D17
17	D16
18	D15
19	D14
20	D13
21	D12
22	D11
23	D10
24	D9
25	RS
26	CSB
27	RDB
28	WRB
29	RESETB
30	VSS
31	VDD
32	VSSH
33	VDDH
34	VSDH
35	NC



SCALE 40 : 1

- NOTES:
- 1.DRIVE IC: SEPS525
  - 2.Die Size : 19660um X 1850um
  - 3.CDF Number : SEPS525\_F00
  - 4.Interface :6/8/9/bit,6bit-RGB, 68XX/80XX Parallel,4-wire SPI

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DRAWN BY:	BY:	TITLE: DLC0169ANOF	SCALE:
CHECKED BY:	BY:	DWG NO:	UNIT: mm
APPROVED BY:	BY:	DWG NAME:	SHEET NO: 0P
CONFIRMED BY:	BY:		

## 5. Interface signals

No	Symbol	Description	Remarks						
1	NC	No Connection							
2	VSDH	Data Driver Ground							
3	VDDH	<i>Data, Scan Driver Power Supply.</i>							
4	VSSH	Scan Driver Ground							
5	IREF	Current Reference for Brightness Adjustment Tie 68K $\Omega$ resistor to VSS.							
6	OSCA2	Fine adjustment for oscillation							
7	OSCA1	Tie 10 K $\Omega$ resistor to OSCA1 between OSCA2. When the external clock mode is selected, OSCA1 is used external clock input.							
8	VDDIO	MPU I/F PAD Power Supply							
9	VSYNCO	RGB Mode Functional Pins							
10	VSYNC	VSYNC: Vertical Sync. Output							
11	HSYNC	VSYNC: Vertical Sync. Input							
12	DOTCLK	HSYNC: Horizontal Sync. Input							
13	ENABLE	DOTCLK: Dot Clock Input ENABLE: Video Enable Input							
14	CPU	<i>Selects the CPU type</i> Low: 80-series CPU, High: 68-Series CPU.							
15	PS	<i>Selects parallel/Serial interface type</i> Low: serial, High: parallel							
16-24	D17-D9	Host Data Input/Output Bus These pins are 9-bit bi-directional data bus to be connected with MCU data bus.							
		<table border="1"> <thead> <tr> <th>PS</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>8_bit bus : D[17:10] 9_bit bus : D[17:9]</td> </tr> <tr> <td>0</td> <td>D[17] SCL : Synchronous clock input D[16] SDI : Serial data input D[15] SDO : Serial data output</td> </tr> </tbody> </table>	PS	Description	1	8_bit bus : D[17:10] 9_bit bus : D[17:9]	0	D[17] SCL : Synchronous clock input D[16] SDI : Serial data input D[15] SDO : Serial data output	
		PS	Description						
		1	8_bit bus : D[17:10] 9_bit bus : D[17:9]						
0	D[17] SCL : Synchronous clock input D[16] SDI : Serial data input D[15] SDO : Serial data output								
	Fix unused pins to the VSS level.								
25	RS	Selects the data/command Low: command, High: parameter/data							
26	CSB	Chip Select Low: SEPS525 is selected and can be accessed. High: SEPS525 is not selected and cannot be accessed.							
27	RDB	Read or Read/Write Enable 80-system bus interface: read strobe signal (active low). 68-system bus interface: bus enable strobe (active high). When serial mode, fix it to VDD or VSS level.							
28	WRB	Write or Read/Write Select 80-system bus interface: write strobe signal (active low). 68-system bus interface: read/write select. Low: write, High: read. When serial mode, fix it to VDD or VSS level							
29	RESETB	Chip Reset Reset SEPS525 (active low)							
30	VSS	Logic Ground							
31	VDD	Logic Power Supply.							

32	VSSH	Scan Driver Ground	
33	VDDH	<i>Data, Scan Driver Power Supply.</i>	
34	VSDH	Data Driver Ground	
35	NC	No Connection	

## 6. Absolute maximum Ratings

### 6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	4.0	V	
supply Voltage for I/O pins	VDDIO	-0.3	4.0	V	
Driver supply voltage	VDDH	-0.3	19.5	V	

### 6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-30	70	°C	
Storage Temperature	TSTG	-40	80	°C	

## 7. Electrical Specifications

### 7.1 Electrical characteristics

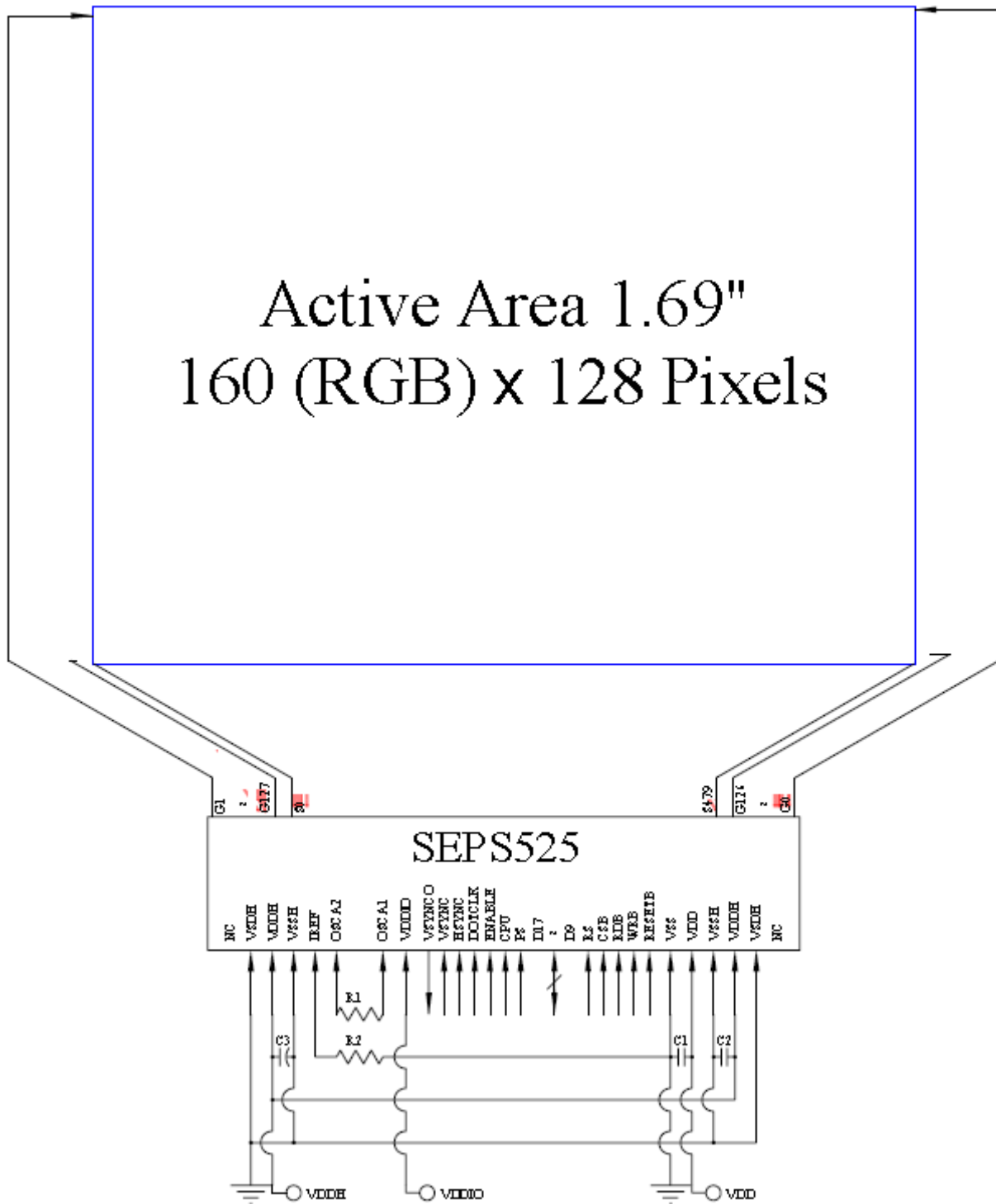
GND=0V, Ta=25°C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	2.6	2.8	3.3	V	
supply Voltage for I/O pins	VDDIO	1.6	2.8	3.3	V	
Driver supply voltage	VDDH	13.5	14.0	14.5	V	
Input Signal Voltage	VIL	0	--	0.4	V	
	VIH	0.8VDD	--	VDD	V	
output Signal Voltage	VOL	-	-	0.4	V	
	VOH	VDD-0.4	-	=	V	
Operating Current for VDD	IVDD	--	2.5	3.5	mA	Note 1
		--	2.5	3.5	mA	Note 2
Operating Current for VDDH	IVDDH	--	25	31	mA	Note 1
		--	8	10	mA	Note 2
Sleep Mode Current for VDD	IVDD, SLEEP	-	1	5	μA	
Sleep Mode Current for VDDH	IVDDH, SLEEP	-	1	5	μA	

Note1: VDD & VDDIO = 2.8V, VDDH = 14V, L<sub>br</sub> @ 100cd/m<sup>2</sup>, full white with polarizer, software initial setting follow section 4.4.2 Reference Parameter

Note 2: VDD & VDDIO = 2.8V, VDDH = 14V, L<sub>br</sub> @ 30cd/m<sup>2</sup>, full white with polarizer, software initial setting follow section 4.4.2 Reference Parameter

7.2 Schematic of OLED module system





## 8. Command/AC Timing

### 8.1 68XX-Series MPU Parallel Interface Timing Characteristics

#### 8.1.1 WRITING TIMING

(VDD = 2.8V, Ta = 25°C)

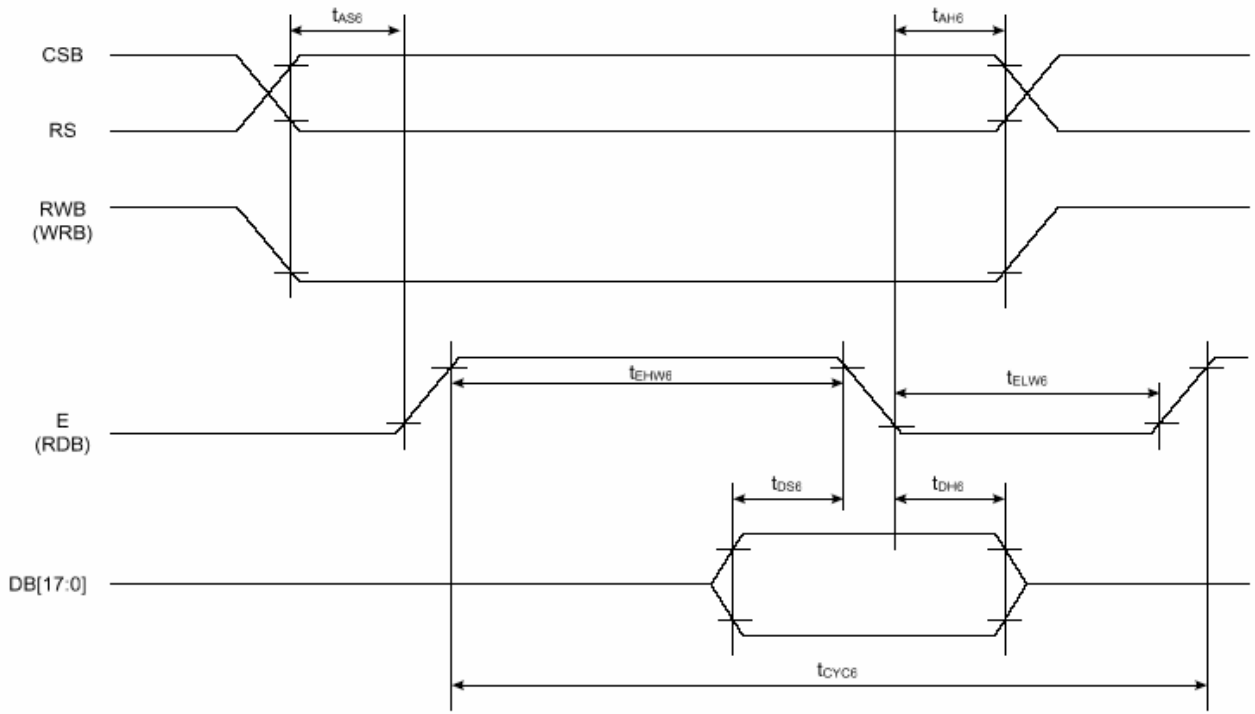
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing	tAH6	5				CSB
Address setup timing	tAS6	5		-	ns	RS
System cycle timing	tCYC6	100				
Write "L" pulse width	tELW6	45			ns	
Write "H" pulse width	tEHW6	45				
Data setup timing	tDS6	40				
Data hold Timing	tDH6	10		-	ns	DB[17:0]

#### 8.1.2 READ TIMING

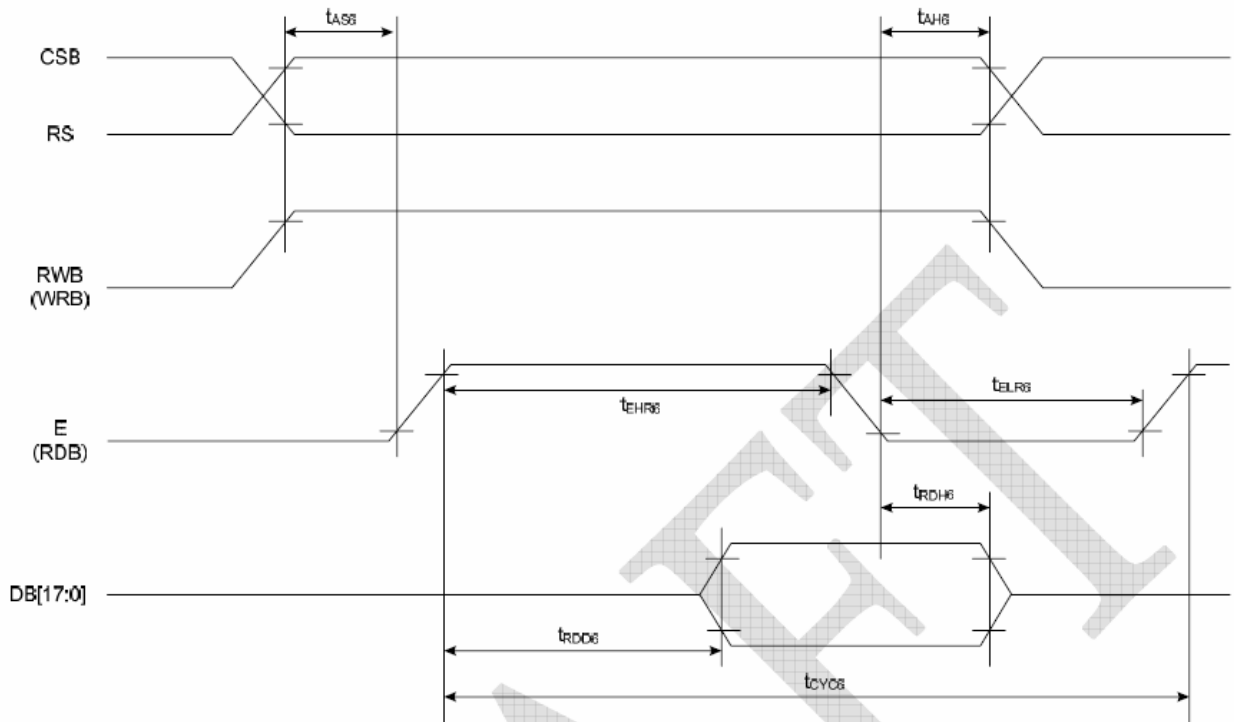
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing	tAH6	10				CSB
Address setup timing	tAS6	10		-	ns	RS
System cycle timing	tCYC6	200				
Read "L" pulse width	tELW6	90			ns	
read "H" pulse width	tEHW6	90				
Data setup timing	trdd6	0		70	ns	CL = 15pF
Data hold Timing	tedh6					DB[17:0]

All the timing reference is 10% and 90% of VDD.

( Write Timing )



( Read Timing )



**8.2 80XX-Series MPU Parallel Interface Timing Characteristics**
**8.2.1 WRITING TIMING**

(VDD = 2.8V, Ta = 25°C)

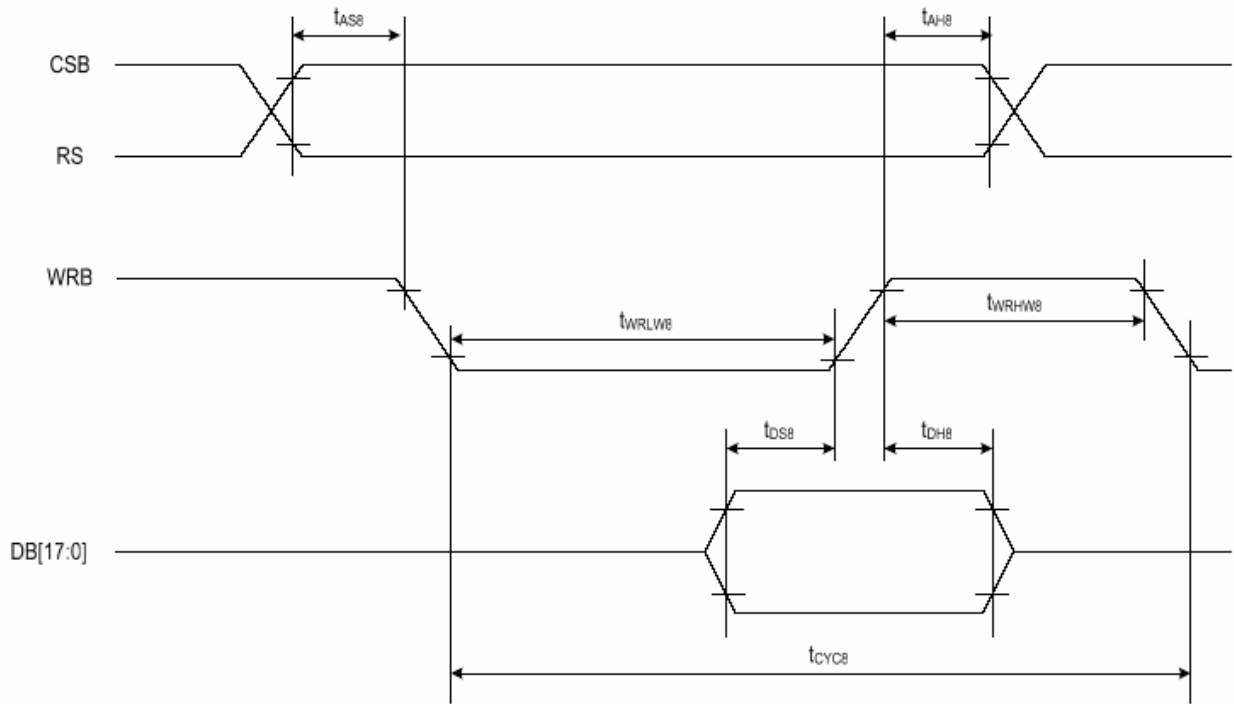
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing	tAH8	5		-	ns	CSB
Address setup timing	tAS8	5				RS
System cycle timing	tCYC8	100				
Write "L" pulse width	tELW8	45			ns	WRB
Write "H" pulse width	tEHW8	45				
Data setup timing	tDS8	30		-	ns	DB[17:0]
Data hold Timing	tDH8	10				

**8.2.2 READ TIMING**

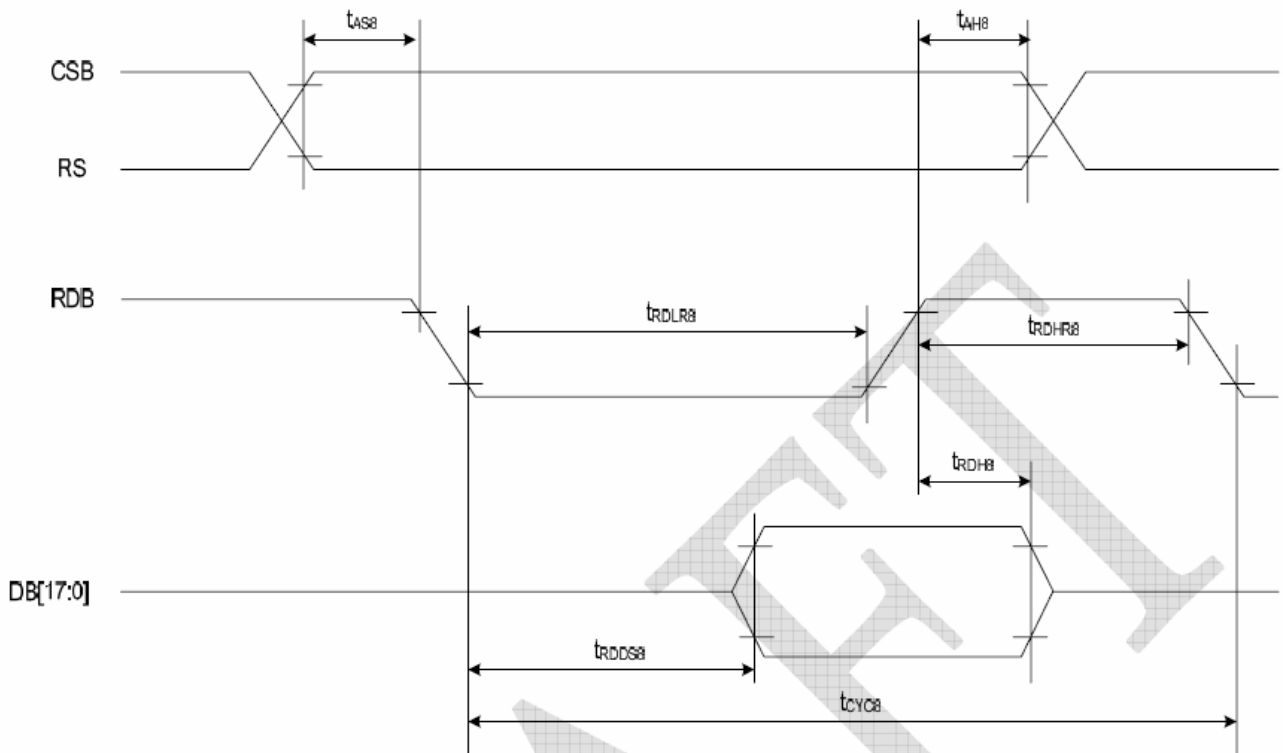
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing	tAH8	10		-	ns	CSB
Address setup timing	tAS8	10				RS
System cycle timing	tCYC8	200				
Read "L" pulse width	tELW8	90			ns	RDB
read "H" pulse width	tEHW8	90				
Data setup timing	Trdd8	0		60	ns	CL = 15pF
Data hold Timing	Tedh8					DB[17:0]

All the timing reference is 10% and 90% of VDD.

( Write Timing )



( Read Timing )

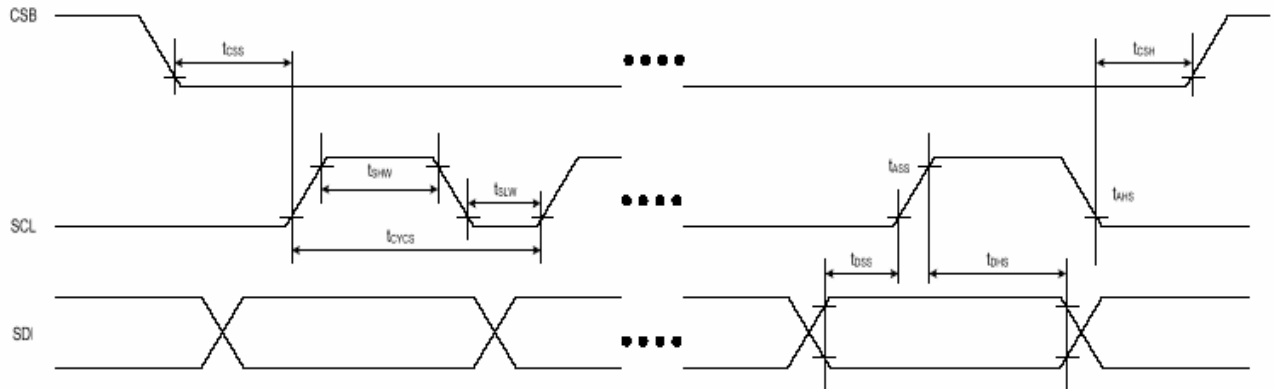


8.3 AC Characteristics INTERFACE

(VDD = 2.8V, Ta = 25°C)

Item	Symbol	MIN	MAX	Unit	Remark
Serial clock cycle	t <sub>CYCS</sub>	60	-		
SCL "H" pulse width	t <sub>SHW</sub>	25	-	ns	SCL
SCL "L" pulse width	t <sub>SLW</sub>	25	-		
CSB-SCL timing	t <sub>css</sub>	25	-	ns	CSB
CSB-hold timing	t <sub>CSH</sub>	25	-		
Data setup timing	t <sub>DSS</sub>	25	--	ns	SDI
Data hold Timing	t <sub>DHS</sub>	25	--		

NOTE: All the timing reference is 10% and 90% of VDD



9. Optical Specification

Ta=25°C

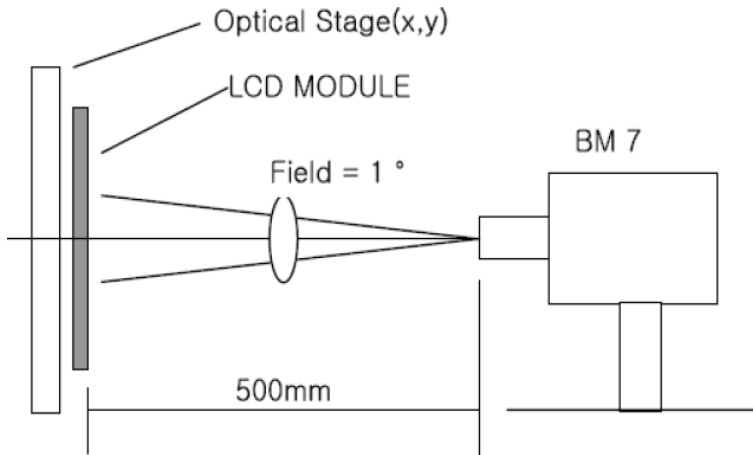
Item	Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	$\theta=0^\circ$		1000	-		Note1 Note2
View Angles	$\theta T$	$CR \geq 2$	80		-	Degree	Note 3
	$\theta B$		80		-		
	$\theta L$		80		-		
	$\theta R$		80		-		
Chromaticity	White	Brightness is on	Typ-0.04	Typ+0.04	0.26		Note4, Note1
					0.28		
	Red				0.65		
					0.34		
	Green				0.30		
					0.62		
	Blue				0.14		
					0.19		
Luminance	L		70	100	-	cd/m <sup>2</sup>	Note1 Note5

Note : Optical measurement with polarizer is taken @ VDD, VDDIO = 2.8V, VDDH = 14V, and the software initial setting with section 4.4.2 Reference

**Note 1: Definition of optical measurement system.**

Temperature = 25°C(±3°C)

LED back-light: ON, Environment brightness < 150 lx

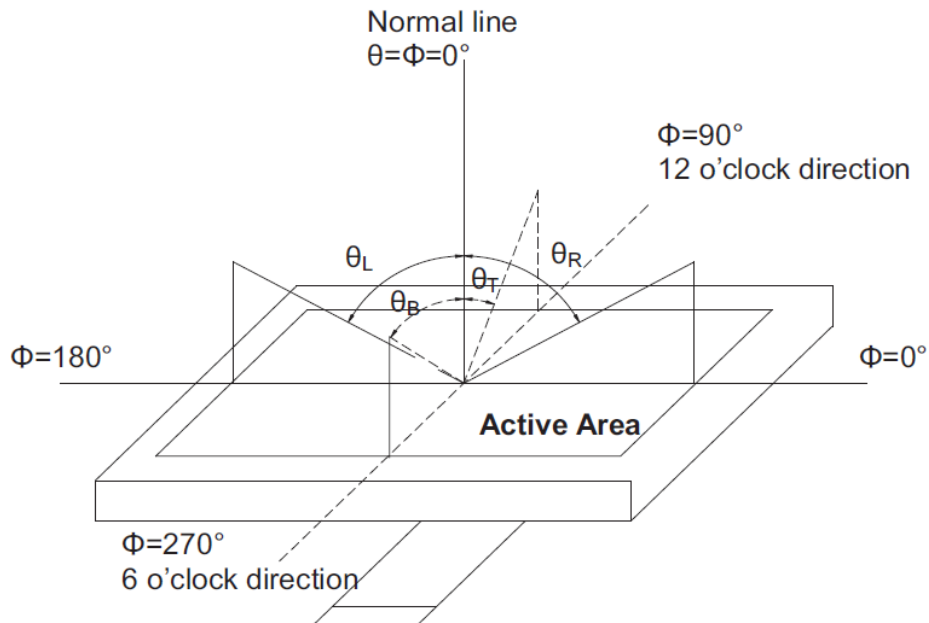


**Note 2: Contrast ratio is defined as follow:**

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

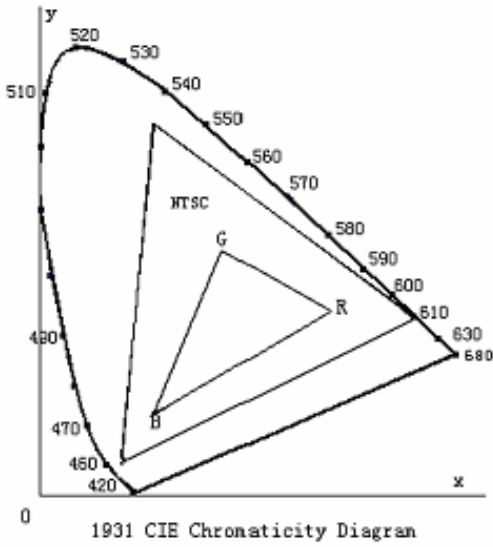
**Note 3: Viewing angle range is defined as follow:**

Viewing angle is measured at the center point of the OLED.



Note 4: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of OLED.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 5: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.



## 10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70°C, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20°C, 120hrs	Per table in below
3	High Temp Storage	Ta=+80°C, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30°C, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+40°C, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30°C 30 min~+80°C 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω · 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

## 11. Precautions for Use of OLED Modules

### 11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

### 11.2 Handling

- A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
- C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
- D. Provide a space so that the panel does not come into contact with other components.
- E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
- F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
- G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
- H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

### 11.3 Static Electricity

- A. Ground soldering iron tips, tools and testers when they are in operation.
- B. Ground your body when handling the products.
- C. Power on the OLED module before applying the voltage to the input terminals.
- D. Do not apply voltage which exceeds the absolute maximum rating.
- E. Store the products in an anti-electrostatic bag or container.

### 11.4 Storage

- A. Store the products in a dark place at  $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$  with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
- B. Storage in a clean environment, free from dust, active gas, and solvent.

### 11.5 Cleaning

- A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
- B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

### 11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

