DLC Display Co., Limited

德爾西顯示器有限公司

MODEL No: DLC0127ANOF

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Record of Revision

Date	Revision No.	Summary
2009-10-28	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0127ANOF, passive matrix OLED module. It is composed of an OLED panel, driver ICs. The 1.27′′ display area contains 128(RGB) x 96 pixels.

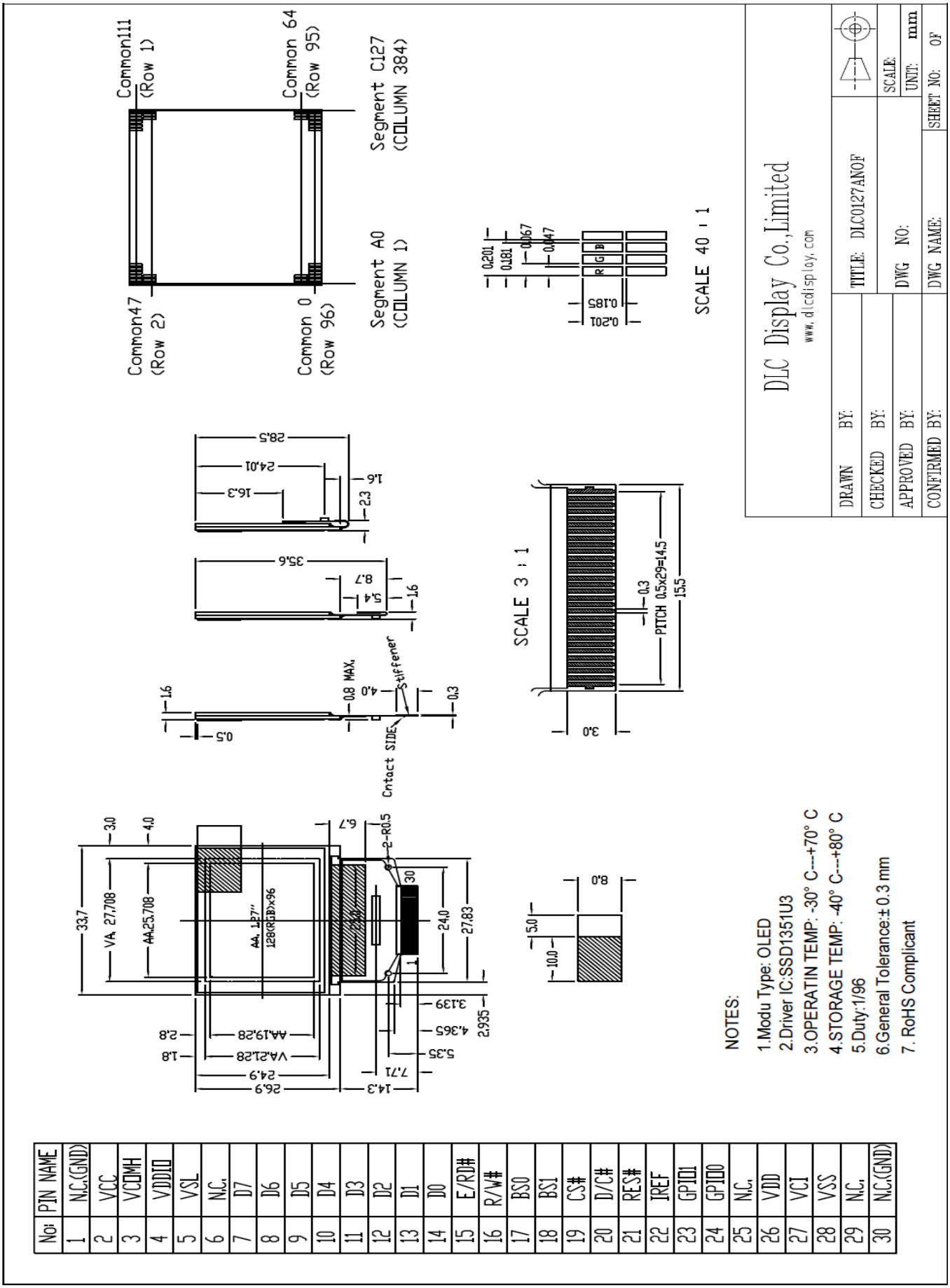
2. Application

Digital equipments which need color display, mobile phone, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	1.27	inch
Resolution	128(RGB) x 96	/
Technology type	Passive OLED	/
Display Color	262,144 Colors (Maximum)	
Interface	8-bits 68XX/80XX Parallel, 3-/4-wire SPI	
Pixel pitch	0.067x0.201	mm
Pixel Configuration	R.G.B. Vertical Stripe	
Outline Dimension (W x H x D)	39.90 ×26.90 × 1.60	mm
Active Area	25.708 × 19.28	mm
Drive Duty	1/96 Duty	/
Driver IC	SSD1351U3	
Operating Temperature	-30℃~+70℃	
Storage Temperature	-40℃~＋80℃	

4. Outline Drawing



No:	PIN NAME
1	N.C.(GND)
2	VCC
3	VCOMH
4	VDDIO
5	VSL
6	N.C.
7	D7
8	D6
9	D5
10	D4
11	D3
12	D2
13	D1
14	D0
15	E/RD#
16	R/W#
17	BS0
18	BS1
19	CS#
20	D/C#
21	RES#
22	IREF
23	GPIO1
24	GPIO0
25	N.C.
26	VDD
27	VCI
28	VSS
29	N.C.
30	N.C.(GND)

5. Interface signals

5.1Pin Definition

Pin Number	Symbol	Type	
Power Supply			
27	VCI	P	Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
26	VDD	P	Power Supply for Core Logic Circuit This is a voltage supply pin which is regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
4	VDDIO	P	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.
28	VSS	P	Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
2	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.
Driver			
22	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5uA.
3	VCOMH	P	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	VSL	P	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
External IC Control			
24 23	GPIO0 GPIO1	I/O	General Purpose Input/Output These pins could be left open individually or have signal inputted/outputted. They are able to use as the external DC/DC converter circuit enabled/disabled control or other applications.

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>17
18</td><td>BS0
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>68XX-parallel (8-bit)</td><td>1</td><td>1</td></tr>
<tr><td>80XX-parallel (8-bit)</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>21</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>20</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data.
When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When 3-wire serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>7~14</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
Unused pins must be connected to VSS except for D2.</td></tr>
</table>

Pin Number	Symbol	I/O	Function
Reserve			
6, 25, 29	N.C.	-	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design
1, 30	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.5	2.75	V	
supply Voltage for I/O pins	VDDIO	-0.5	VCI	V	
Supply Voltage for Operation	VCI	-0.3	4	V	
Supply Voltage for Display	VCC	-0.5	16	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-30	70	℃	
Storage Temperature	TSTG	-40	80	℃	

7. Electrical Specifications

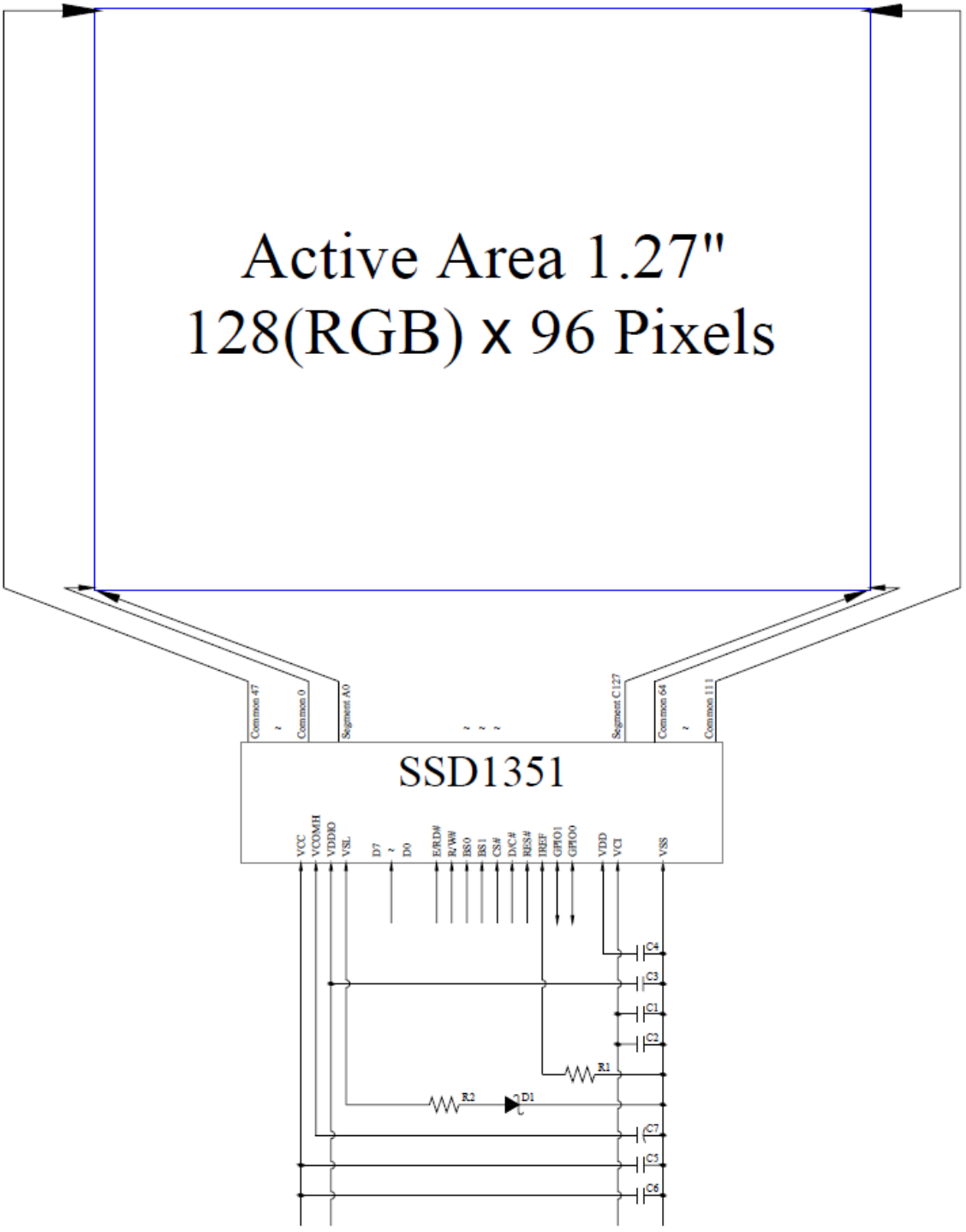
7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	2.4	2.5	2.6	V	
supply Voltage for I/O pins	VDDIO	1.65	1.8	VCI	V	
Supply Voltage for Operation	VCI	2.4	2.8	3.5	V	
Supply Voltage for Display	VCC	11.5	12	12.5	V	Note1
Input Signal Voltage	VIL	0	--	$0.2 \times V_{DDIO}$	V	
	VIH	$0.8 \times V_{DDIO}$	--	V_{DDIO}	V	
Output Signal Voltage	VOL	0	-	$0.1 \times V_{DDIO}$	V	
	VOH	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V	
Operating Current for VCI	ICI	--	240	300	μA	
Operating Current for VCC	ICC	--	16.1	20.1	mA	Note 2
		--	27.0	33.8	mA	Note 3
Sleep Mode Current for VCI	ICI, SLEEP	-	1	5	μA	
Sleep Mode Current for VCC	ICC, SLEEP	-	1	5	μA	

Note 1: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.
Note 2: VCI = 2.8V, VCC = 12V, 50% Display Area Turn on.
Note 3: VCI = 2.8V, VCC = 12V, 100% Display Area Turn on.

7.2 Schematic of OLED module system



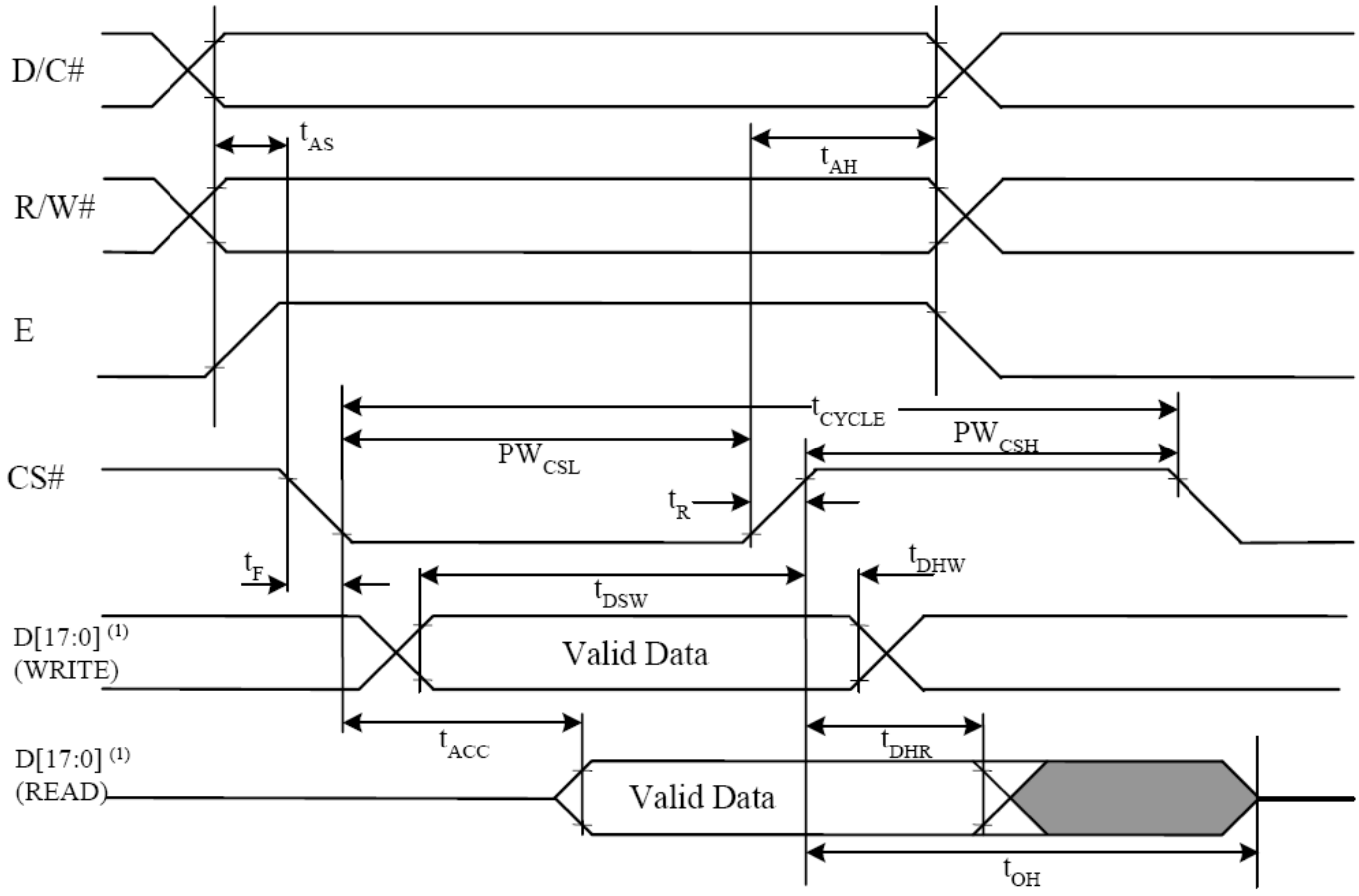
MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#
C1, C5: 0.1μF
C2: 4.7μF
C6: 10μF
C3, C4: 1μF
C7: 4.7uF / 25V Tantalum Capacitor
R1: 560kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

8. Command/AC Timing

8.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.65V, VCI = 2.8V, Ta = 25°C)

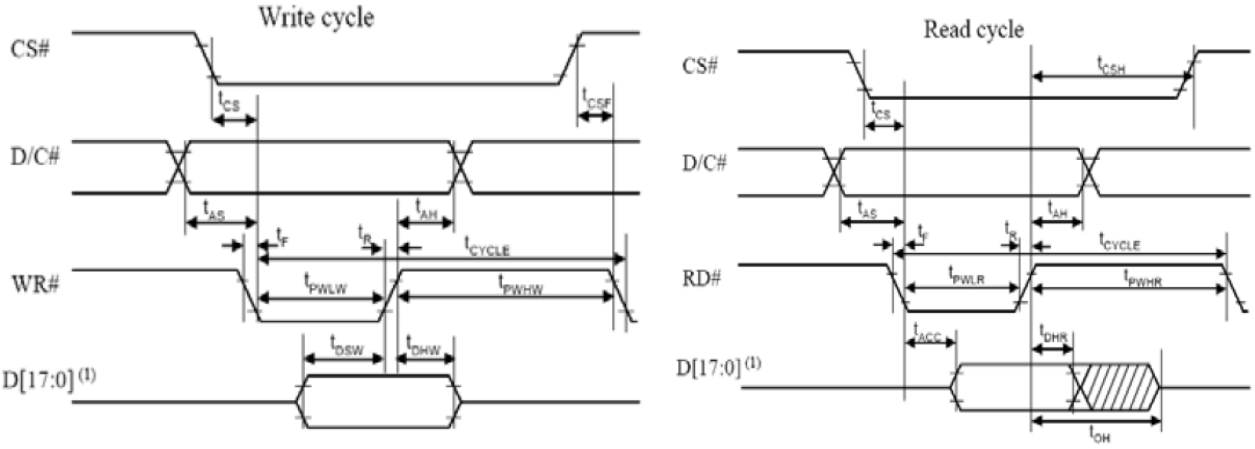


When 8-bit Used: D[7:0] Instead

8.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.65V, VCI = 2.8V, Ta = 25°C)

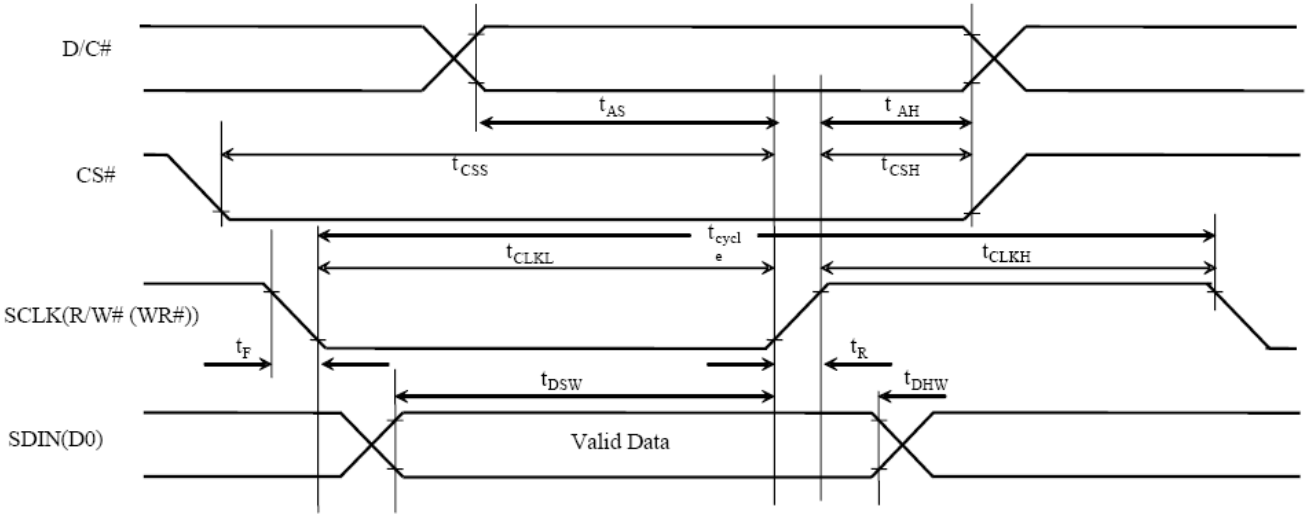


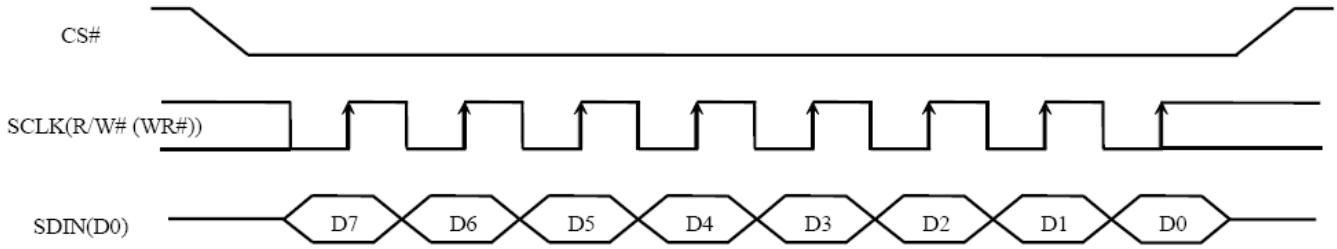
(1) When 8-bit Used: D[7:0] Instead

8.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15		ns
t_{DHW}	Write Data Hold Time	15		ns
t_{CLKL}	Clock Low Time	20		ns
t_{CLKH}	Clock High Time	20		ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.65V, VCI = 2.8V, Ta = 25°C)

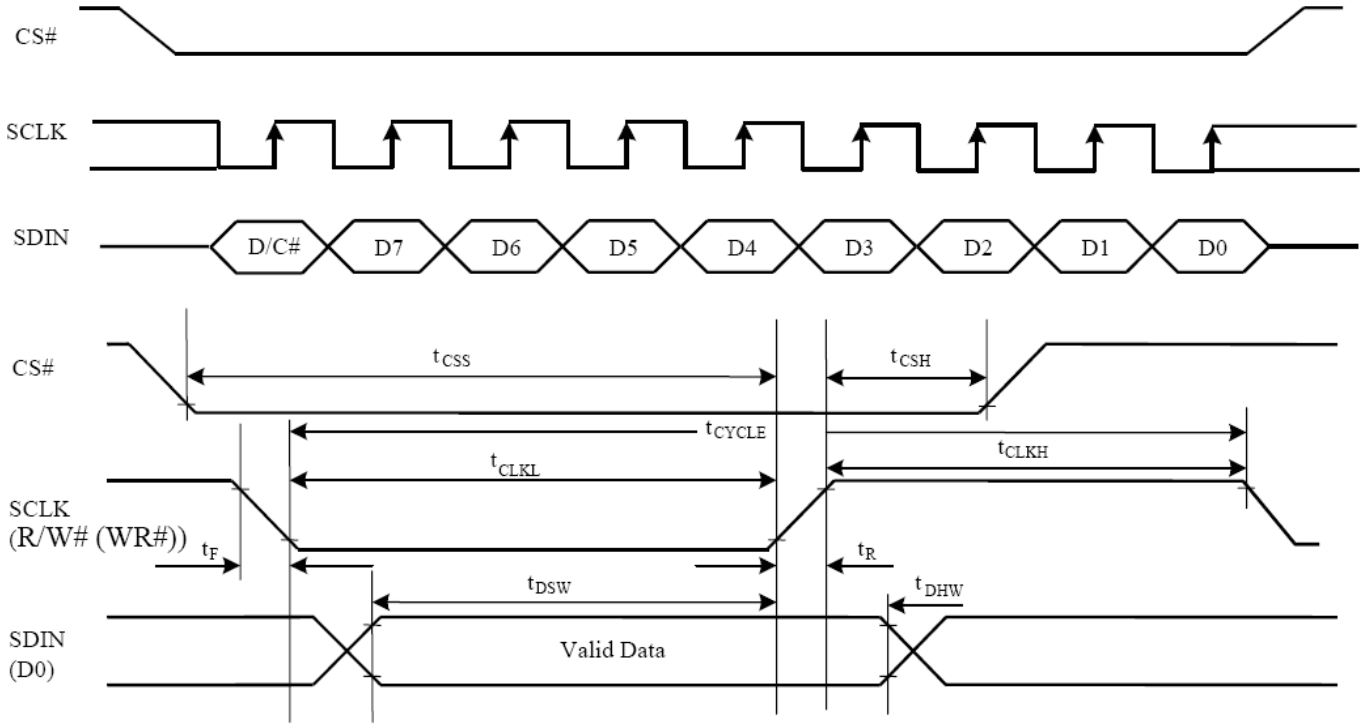




8.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20		ns
t_{CLKH}	Clock High Time	20		ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

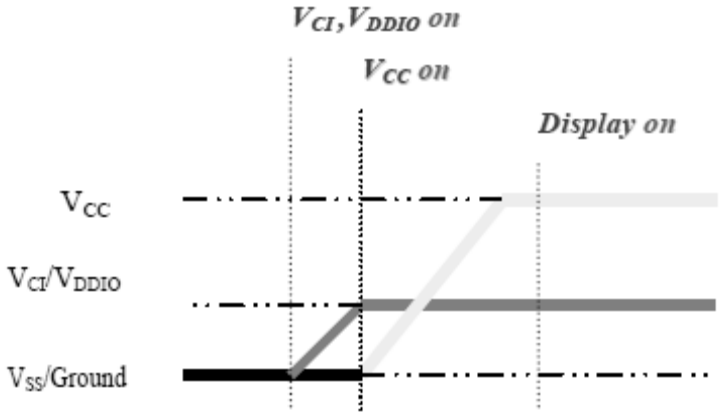
(VDD - VSS = 2.4V to 2.6V, VDDIO = 1.65V, VCI = 2.8V, Ta = 25°C)



8.5 Power down and Power up Sequence

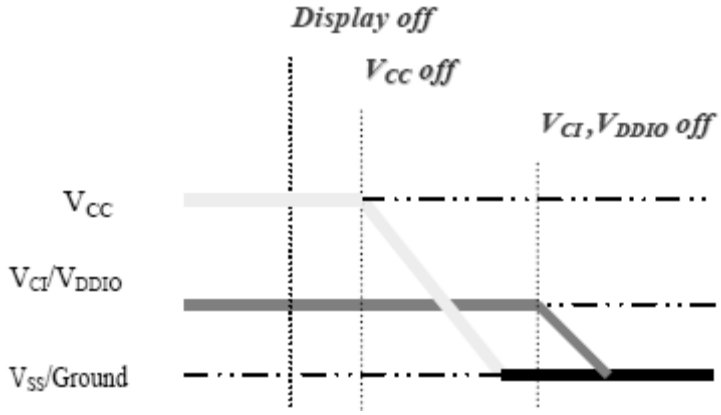
Power up Sequence:

1. Power up VCI & VDDIO
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 100ms(when VCC is stable)
7. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms(when VCC is reach 0 and panel is completely discharges)
4. Power down VCI & VDDIO



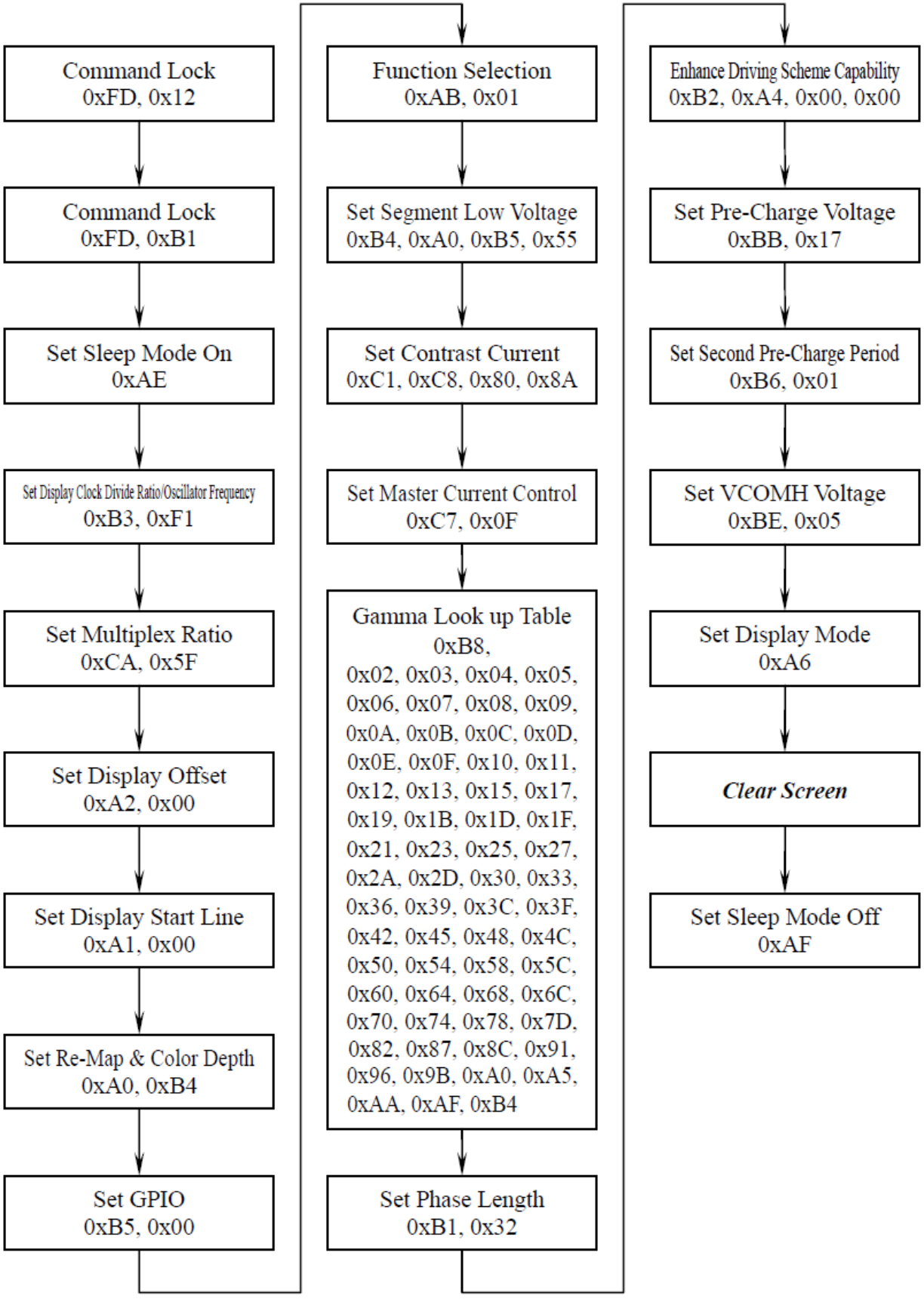
8.6 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128(RGB)×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Command A2h, B1h, B3h, BBh, BEh are locked by command FDh

8.7 Actual Application Example

<Initialization>



9. Optical Specification

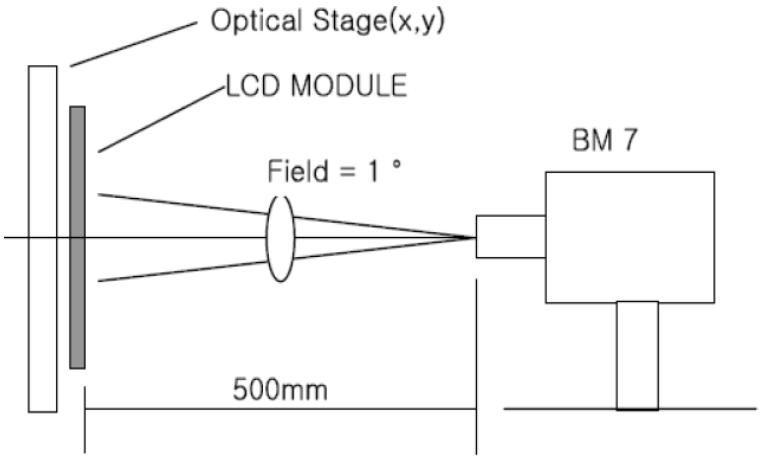
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°		2000	-		Note1 Note2
View Angles		ΘT	--	160		-	Degree	Note 3
Response time	Rise	Tr	--	-	-	0.02	ms	Note 4
	Decey	Td	--	-	-	0.02	ms	
Chromaticity	White	x		0.26	0.30	0.34		Note 5
		y		0.29	0.33	0.37		
	Red	x		0.60	0.64	0.68		
		y		0.30	0.34	0.38		
	Green	x		0.27	0.31	0.35		
		y		0.58	0.62	0.66		
	Blue	x		0.10	0.14	0.18		
		y		0.12	0.16	0.20		
Luminance		L	--	80	100	-	cd/m^2	Note1 Note6
Operating Life Time		Top	L＝100cd/m2	10000			Hours	Note7

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

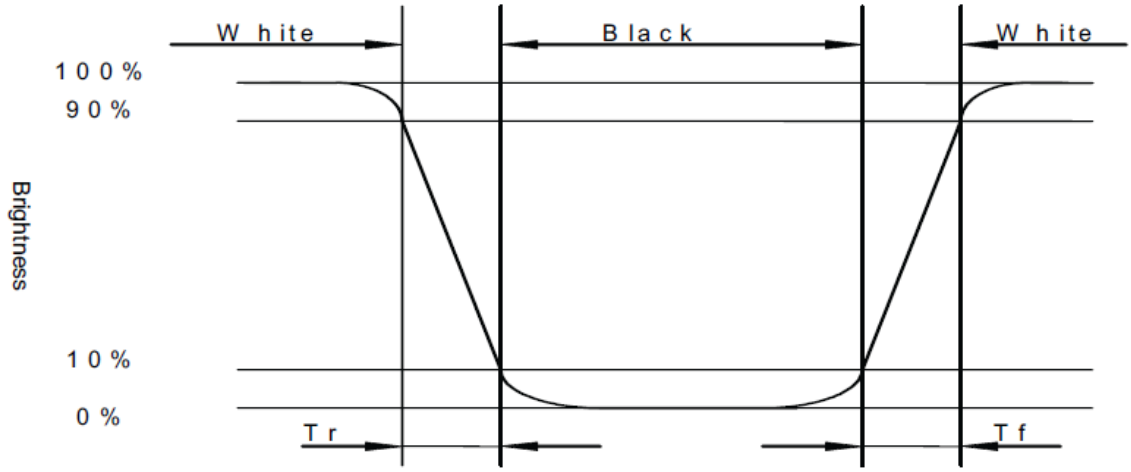


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

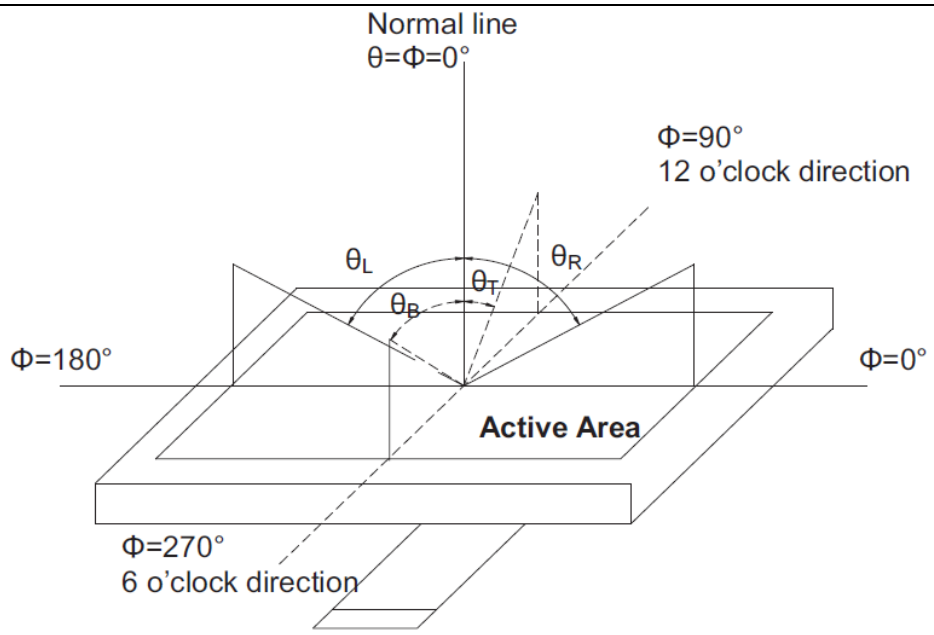
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



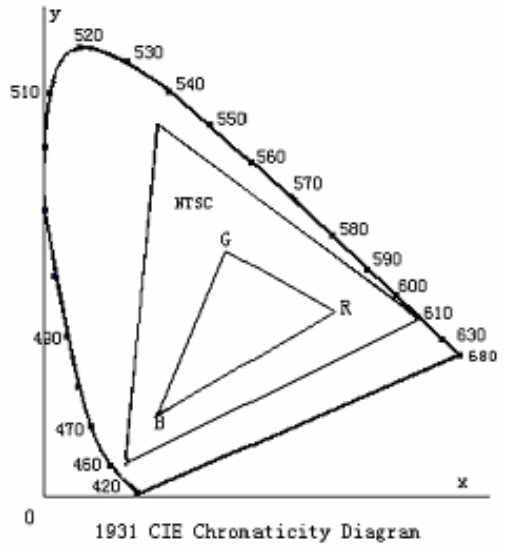
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 7: Life Time is defined as follow:

When the Luminance has decayed to less than 50% of the initial Luminance specification. (50% pixels scrolling display on) (The initial value should be closed to the typical value after adjusting.)

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 240hrs	The operational functions work.
2	Low Temp Operation	Ta=-30℃, 240hrs	The operational functions work.
3	High Temp Storage	Ta=+80℃, 240hrs	The operational functions work.
4	Low Temp Storage	Ta=-40℃, 240hrs	The operational functions work.
5	High Temp & High Humidity Storage	Ta=+40℃, 90% RH 120 hours	The operational functions work.
6	Thermal Shock (Non-operation)	-40°C ~ 85°C, 24 cycles 60 mins dwell	The operational functions work.
7	ESD (Operation)	C=150pF, R=330Ω , 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.